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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/540,163	03/31/2000	Carlos H. Morales	ADAPP137	2702

25920 7590 07/13/2004

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EXAMINER	
TRAN, ELLEN C	

ART UNIT	PAPER NUMBER
2134	5

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/540,163	MORALES, CARLOS H.	
	Examiner	Art Unit	
	Ellen C Tran	2134	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

NORMAN M. WRIGHT
PRIMARY EXAMINER

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

1 This action is responsive to communication: amendment filed on 27 April 2004, the original application was filed on 31 March 2000.

2. Claims 1-24 are currently pending in this application. Claims 1, 14, and 21 are independent claims.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1 and 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Riley et al. U.S. Patent No. 6,266,731 (hereinafter '731), in view of Schwaderer white paper "Domain Validation Explained" (hereinafter Schwaderer).

As to independent claim 1, "A method for verifying bus performance in a multiple initiator environment" is taught in '731 col. 12, lines 17-32 "present invention, Registered PCI introduces several major enhancements ... such that devices can signal 2 blocks before an expected response from other devices with the least impact to bus performance ... New information passed with each transaction that enables more efficient buffer management schemes";

"a first initiator implementing the method, comprising: generating a key data pattern including a key header and a pattern" is disclosed in '731 col. 12, lines 36-40 "Each transaction includes the identity of the initiator (Initiator Number), the initiator's bus segment (Bus Number) and transaction sequence (or "thread") to which it belongs (Sequence Number);

"reading the key data pattern; and examining the key header to ascertain a level of communication integrity of a physical connection with the target" is shown in '731 col. 12, lines 36-40 "An extended command field further qualifies each transaction";
the exact terminology of "writing the key data pattern to an echo buffer of a target" **is not disclosed in '731 however** Schwaderer discloses "Echo Buffer: An optional 252 character buffer located on a target device" page 1, last paragraph.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the teachings of '731, a SCSI bus monitoring system to include an echo buffer. One of ordinary skill in the art would have been motivated to perform such a modification as indicated by Schwaderer (see page 1 last sentence.) "An echo buffer helps its device perform enhanced Domain Validation procedures".

As to independent claim 14, "A computer implemented method for verifying bus performance in a multiple initiator environment that includes at least a first initiator and a second initiator in communication with a target device" is taught in '731 col. 12, lines 17-32 "present invention, Registered PCI introduces several major enhancements ... such that devices can signal 2 blocks before an expected response from other devices with the least impact to bus performance ... New information passed with each transaction that enables more efficient buffer management schemes";

"the method comprising: generating a key data pattern; is disclosed in '731 col. 12, lines 36-40 "Each transaction includes the identity of the initiator (Initiator Number), the initiator's bus segment (Bus Number) and transaction sequence (or "thread") to which it belongs (Sequence Number);

"sending a write echo buffer (VVEB) command to write the key data pattern to an echo buffer of the target" is disclosed in Schwaderer page 2, col. 2 "Here, the initiator transmits the data using the Write Buffer command with the echo buffer option";

"sending a read echo buffer (REB) command to the echo buffer, the REB command being configured to request a transmission of the key data pattern from the echo buffer to the first initiator" is disclosed in Schwaderer page 2, col. 2 "and request it back using the Read Buffer command with the echo buffer option";

"and examining the key data pattern received from the echo buffer to ascertain a level of communication integrity of a physical Connection between the first initiator and the target device" is shown in '731 col. 12, lines 36-40 "An extended command field further qualifies each transaction".

5. **Claims 2-4, 18-21, 23, and 24** are rejected under '731 and Schwaderer as applied to claims 1 and 14 in view of Kwan et al., U.S. Patent No. 6,658,459 (hereinafter '459).

As to dependent claims 2 and 18 "A method for verifying bus performance in a multiple initiator environment as recited in claim ..., wherein generating the key header includes: generating a byte 0; generating a byte 1; generating a byte 2; and generating a byte 3" **the exact terminology is not disclosed in the combination of '731 and Schwaderer however '459 discloses** "The translation adapter 210 first looks for a 16-byte header, and then validates

the header by examining an 8-byte SCSIHubId field for a "SCSIHUB" signature. From the information contained in the 8-byte SCSIHubId field, the translation adapter 210 can determine the data type, the direction, and the size of the subsequent data transfer, and then act upon the information" in col. 7 line 65 thru col. 8 line 4.

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination of teachings of '731 and Schwaderer, a SCSI bus monitoring system with an echo buffer to include a byte header. One of ordinary skill in the art would have been motivated to perform such a modification because defining the byte header is just one aspect taught in '459 to enable sharing of peripheral devices. As indicated by '459 (see col. 2, lines 31 et seq.) "Broadly speaking, the present invention fills these needs by providing a method, a system and an apparatus for transparently sharing remotely networked peripheral devices with local client computers".

As to independent claim 21, "A computer readable media having program instructions for" is disclosed in '459 (col. 11 lines 50 et seq.) "The invention can also be embodied as computer readable code on a computer readable medium" the remainder of the claim has the same limitation as explained and rejected above in claim 1 and 14.

As to dependent claim 23, is rejected using the same rationale as cited above.

As to dependent claims 3, 19, and 24 "A method for verifying bus performance in a multiple initiator environment as recited in claim ..., wherein the byte 0 is an ID byte, the byte I is a host ID," is disclosed in '731 col. 12, lines 32-40 "Each new transaction identifies the total number of bytes that will be read or written, even if the transaction is disconnected and continued later. Each transaction includes the identity of the initiator (Initiator Number), the

initiator's bus segment (Bus Number) and transaction sequence (or "thread") to which it belongs (Sequence Number)";

"the byte 2 is a logical negation of the host ID, and byte 3 is a logical negation of the ID byte" An extended command field further qualifies each transaction" col. 13 lines 5-11 "The initial transaction of each operation is marked so the target knows when to flush buffers containing stale data. Target devices of read operations can use this information to optimize prefetch and buffer management algorithms".

As to dependent claim 4 and 20, "A method for verifying bus performance in a multiple initiator environment as recited in claim ..., wherein the ID byte is a manufacturer signature ID, and the host ID is an initiator ID" is disclosed in '459 col. 9, lines 29-34 "then reads a 16-byte header to determine if the packet is intended for the translation adapter. Once the 16-byte header has been read, an 8-byte SCSIHubId header is examined in order to validate the SCSIHUB signature".

6. **Claims 5-7 and 22** are rejected under 35 U.S.C. 103(a) as being unpatentable over '731 and Schwaderer as applied to claims 1 and 21 in view of '459, further in view of Regis U.S. Patent No. 6,405,272 (hereinafter '272).

As to dependent claim 5 and 22, "A method for verifying bus performance in a multiple initiator environment as recited ... wherein examining the key header includes one of: determining whether the echo buffer returns an error indication" is taught in '731 col. 24 lines 34-37 "If a device receiving data detects a data parity error, it shall assert PERR# on the second clock after PAR is asserted (1 clock later than conventional PCI)";

The following in italics is not taught in exact terminology of the combination of teachings in '731 and'459.

"determining whether data of the key header has been changed" is disclosed in '272 col. 9, lines 63-66 "wherein said monitoring observes, bit-by-bit, whether a signal level on said arbitration line corresponds to said processing module's address";

"or determining whether the data in the key header specifically indicates a collision with data from another initiator using a same key header system" is disclosed in '272 col. 9, lines 54-56 "while monitoring said arbitration line to detect for collisions on said arbitration line".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination teachings of '731, Schwaderer, and '459 a SCSI bus monitoring system with an echo buffer using byte header to include bus arbitration. One of ordinary skill in the art would have been motivated to perform such a modification because bus arbitration is needed to for a system with competing processing modules. As indicated by '272 (see col. 2, lines 55 et seq.) "A parallel packetized intermodule arbitrated high speed control data bus system is provided which allows high speed communication between microprocessor modules in a more complex digital processing environment".

As to dependent claim 6, "A method for verifying bus performance in a multiple initiator environment as recited in claim 5, wherein the determining of whether data of the key header has been changed occurs when the multiple initiators are heterogeneous" " is disclosed in '272 col. 9, lines 63-66 "wherein said monitoring observes, bit-by-bit, whether a signal level on said arbitration line corresponds to said processing module's address";

As to dependent claim 7, "A method for verifying bus performance in a multiple initiator environment as recited in claim 5, wherein the determining of whether the data in the key header specifically indicates the collision occurs when the multiple initiators are homogeneous" " is disclosed in '272 col. 9, lines 54-56 "while monitoring said arbitration line to detect for collisions on said arbitration line".

7. **Claims 8-13 and 15-17** are rejected under 35 U.S.C. 103(a) as being unpatentable over '731 and Schwaderer as applied to claim 1 and 14, in view of '459, further in view of '272, further in view of Sheth et al. U.S. Patent NO. 5,386,517 (hereinafter '517).

As to dependent claim 8, the combination teachings of '731, '459, and '272 do not include the following in the exact terminology "A method for verifying bus performance in a multiple initiator environment as recited in claim 5, wherein when it is determined that the error indication is returned from the echo buffer, the first initiator being configured to rewrite the key data pattern to the echo buffer, the rewriting being performed for a set number of times before an adjustment is made to the level of communication integrity of the physical connection with the target" is taught in '517 col. 19 lines 14-15 "The retry process will continue until a predetermined retry limit is reached".

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify the combination teachings of '731, '459, and '272 a SCSI bus monitoring system with a byte header with error detection to include a method to retry for a predetermined number of times. One of ordinary skill in the art would have been motivated to perform such a modification because bus management needs several interfacing mechanisms. As indicated by '517 (see col.

1, lines 34 et seq.) "The Input/Output Module Subsystem (IOM) described herein relieves the Central Processing Modules (CPM) of I/O functions thus freeing the CPMs to work on higher priority tasks while the IOM provides rapid throughput for data communication and control to various types of peripheral units".

As to dependent claim 9, "A method for verifying bias performance in a multiple initiator environment as recited in claim 6, wherein when it is determined that the data of the key header has been changed, the first initiator being configured to rewrite the key data pattern to the echo buffer, the rewriting being performed for a set number of times before an adjustment is made to the level of communication integrity of the physical connection with the target" is taught in '517 col. 19 lines 14-15 "The retry process will continue until a predetermined retry limit is reached".

As to dependent claim 10, "A method for verifying bus performance in a multiple initiator environment as recited in claim 7, wherein when it is determined that the data in the key header specifically indicates the collision with data from another initiator using the same key header system" is taught in '272 col. 9, line 63 thru col. 10, line 4 " The arbitration system according to claim 3, wherein said monitoring observes, bit-by-bit, whether a signal level on said arbitration line corresponds to said processing module's address ... The arbitration system according to claim 4, wherein if said signal level is different than-said-shifted-out address bit signal level, said processing module desiring access to the communication bus drops out of contention";

"the first initiator being configured to rewrite the key data pattern to the echo buffer, the rewriting being performed for a set number of times before an adjustment is made to the level of communication integrity of the physical connection with the target" is taught in '517 col. 19 lines 14-15 "The retry process will continue until a predetermined retry limit is reached".

As to dependent claim 11, "A method for verifying bus performance in a multiple initiator environment as recited in claim 7, wherein the collision occurs when a byte 0 matches a specific manufacturer ID, a byte I does not match the first initiator's ID" is taught in '272 col. 5, lines 42-51 "The arbitration method depends on the detection of collisions and uses state machines 46 and 48 within the bus controller 22 on each processing module 34 to determine arbitration bus 50 status as arbitration proceeds. All transitions on the arbitration bus 50 are synchronized to the bus clock 42. Each processor module 34 has a unique programmed binary address to present to the arbitration bus 50. The device address in the current embodiment is six bits, thereby yielding 63 unique processing module 34 identifications";

"a byte 2 is a logical negation of byte 1, and a byte 3 is a logical negation of byte 0" is taught in '272 col. 5, lines 28-35 "As known to those familiar with the art, the connection is called "wired-OR" since it behaves like a large NOR gate with the line going low if any device drives high (DeMorgan's theorem). An active low receiver inverts a logic 0 level, producing an equivalent OR gate. Using positive-true logic conventions yields a "wired-AND," using negative logic yields a "wired-OR." This is used to indicate if at least one device is driving the arbitration bus 50 and does not require additional logic. Therefore, if a processing module 34 asserts a logic 1 on the arbitration bus 50 and monitors a logic 0, via buffer 53 on monitor line 55

(BUS_ACT_N), the processing module 34 bus controller 22 determines that a collision has occurred and that it has lost the arbitration for access".

As to dependent claim 12, "A method for verifying bus performance in a multiple initiator environment as recited in claim 6, wherein when it is determined that data of the key header has been changed, it is assumed that a collision occurred" is taught in '272 col. 5, lines 42-51 "The arbitration method depends on the detection of collisions and uses state machines 46 and 48 within the bus controller 22 on each processing module 34 to determine arbitration bus 50 status as arbitration proceeds. All transitions on the arbitration bus 50 are synchronized to the bus clock 42. Each processor module 34 has a unique programmed binary address to present to the arbitration bus 50. The device address in the current embodiment is six bits, thereby yielding 63 unique processing module 34 identifications".

As to dependent claim 13, "A method for verifying bus performance in a multiple initiator environment as recited in claim 1, wherein writing the key data pattern includes: sending linked commands to the echo buffer to prevent the echo buffer from receiving data from another initiator, the linked commands being configured to link write and read commands and to disable a SCSI disconnection" is disclosed in Schwaderer page 3, 1st paragraph "Having secured the target device for exclusive use, the initiator can echo any and as many data patterns as needed".

As to dependent claim 15, "A computer implemented method for verifying bus performance in a multiple initiator environment as recited in claim 14, wherein before the key data pattern is generated, the method includes: sending an asynchronous inquiry to the target device" is taught in '517 col. 7, lines 22-24 "The MCP passes a Asynchronous Schedule message

containing the IOCB address and a device reference to the IOU 78 via a command designated XFNC";

"the asynchronous inquiry being configured to request a transmission of a valid data pattern from the target device and receiving the valid data pattern from the target device in response to the asynchronous inquiry" is disclosed in '517 col. 7, lines 24-26 "The XFNC operator waits for an "Acknowledge Message" before completing";

"and sending a synchronous inquiry to the target device, the synchronous inquiry being configured to request a faster transmission of another valid data pattern in order to negotiate an optimal throughput speed with the target device and receiving the another valid data pattern from the target device in response to the synchronous inquiry" is taught in '517 col. 5 lines 60-65 "When sending message data out onto the TM bus 42, the data is first trickled into a packet storage buffer located within the interbus module (PMIU) 20IM. Then the message can be returned at the proper timing rate without running into RAM access contention".

As to dependent claim 16, A computer implemented method for verifying bus performance in a multiple initiator environment as recited in claim 15, wherein after the sending of the synchronous inquiry, the method includes: sending a read echo buffer description (REBD) command to the echo buffer of the target, the REBD command being configured to request information regarding a size of the echo buffer and whether the echo buffer supports collision detection" is taught in Schwaderer page 3, 1st paragraph "However, before echoing any data, the initiator must first determine the size of the target device's echo buffer which can vary by device".

As to dependent claim 17, "A computer implemented method for verifying bus performance in a multiple initiator environment as recited in claim 14, further comprising: detecting a data collision during the examining of the key data pattern received from the echo buffer" is disclosed in '272 col. 9, lines 54-56 "while monitoring said arbitration line to detect for collisions on said arbitration line";

"and if a collision is detected, the method includes, re-sending a VVEB command with the key data pattern" and "the re-sending being performed for a set number of times before an adjustment is made to the level of communication integrity of the physical connection between the first initiator and the target" are taught in '517 col. 19 lines 14-15 "The retry process will continue until a predetermined retry limit is reached";

" to the echo buffer" is disclosed in Schwaderer page 1, last paragraph "Echo Buffer: An optional 252 character buffer located on a target device".

Response to Arguments

8. Applicant's arguments filed 27 April 2004 have been fully considered but they are not persuasive.

In response to applicant's argument on page 9, "In contrast independent claims 1, 14, and 21 recite methods and program instructions that "generate a key pattern," which is examined to "ascertain a level of communication integrity" in order to verify bus performance. Bus performance verification is not "device configuration" as disclosed by Riley et al." The office disagree bus performance is inherent in Riley as well as when connecting devices, see Riley col. 5, lines 35-43.

In response to applicant's argument on page 10, "However, combining Schwaderer with a reference that provides motivation for device configuration does not render obvious the claimed invention". The office disagrees Riley teaches "bus performance verification" therefore the reason to combine with Schwaderer is still maintained for writing and reading to an echo buffer. In addition the combination to combine with Kwan is still maintained to for byte header definition.

In response to applicant's argument on page 10, "Riley does not teach or suggest, "examining the key header" ... or suggest the remaining features of the independent claims related to the "examining"". The office disagrees the word "qualifies" in Riley col. 12, lines 36-40 has the meaning as "examining" in the claimed invention.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a). A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ellen C Tran whose telephone number is (703) 305-8917. The examiner can normally be reached on 6:30 am to 3:30 pm Monday - Thursday and alternating Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Gregory A Morse can be reached on (703) 308-4789. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Ellen. Tran
Patent Examiner
Technology Center 2134
1 July, 2004

NORMAN M WRIGHT
PRIMARY EXAMINER